In the Specification

Please amend paragraphs [0004] as follows:

In recent years, flash memory device has become the main stream of the non-volatile memory device since that type of memory device allows_for multiple data writing, loading and erasing operations. In addition, the stored data can be preserved even the power of the memory device is removed.

Please amend paragraphs [0005] as follows:

In a conventional flash memory device, generally the floating gate and control gate of are manufactured with doped amorphous silicon. In a stacked gate_flash memory device, the control gate is disposed on the floating gate directly, a dielectric layer is disposed between the floating gate and the control gate, and a tunnel oxide layer is disposed between the floating gate and the substrate.

Please amend paragraphs [0008] as follows:

Further, the conventional flash memory array includes the NOR_array structure and the NAND array structure. Since in the NAND array structure, the memory cells are connected in series, the integration of the NAND array structure is larger than that of the NOR array structure. However, the writing and the loading procedure of the memory cell of the NAND array structure is more complex. For example, the programming and erase operation of the memory cell of the NAND array structure are all performed by the tunnel F-N (Fowler-Nordheim) tunneling effect, to inject electrons into the floating gate via the tunnel oxide layer, and to pull out electrons from the floating gate to the substrate via the tunnel oxide layer. Therefore, the tunnel oxide layer will be damaged under high voltage

operation and the stability will be reduced. Moreover, since a lot of memory cells are connected in series in the NAND array, the loading current of the memory cell is reduced; thus, the operation speed and the performance of the memory cell are also reduced.

Please amend paragraphs [0009] as follows:

Accordingly, one object of the present invention is to provide a NAND flash memory cell row to enhance the performance of a_memory cell.

Please amend paragraphs [0010] as follows:

Another object of the present invention is to provide a_manufacturing method of NAND flash memory cell row, wherein the manufacturing a NAND flash memory cell row with high erase speed can be simplified.

Please amend paragraphs [0011] as follows:

In order to achieve the above objects and other advantages of the present invention, a NAND flash memory cell row is provided. The NAND flash memory cell row includes_a plurality of first stacked gate structures, second stacked gate structures, control gates, floating gates, an inter-gate dielectric layer, a tunnel oxide, a plurality of doping regions and a plurality of source/drain regions. The first stacked gate structures are disposed on a substrate, and each of the first stacked gate structures_includes an erase gate dielectric layer, an erase gate and a first cap layer. The second stacked gate structures_are disposed on_the substrate beside two outer sides of the first stacked gate structures_respectively, and each of the second stacked gate structures_includes a select gate dielectric layer, a select gate and a second cap layer. The control gate is disposed between the first stacked gate structures and each of the second stacked gate structures,

and between every two of the neighboring first stacked gate structured. The floating gate is disposed between the control gate and the substrate, and has a sharp corner and a concave surface facing each of the control gate. The edge of the concave surface is lower than the top surface of the erase gates. The inter-gate dielectric layer is disposed between each of the control gates and each of the floating gates. The tunnel oxide, disposed between_each of the floating gates and the substrate, between each of the floating gates and the first stacked gate structures, and between each of the floating gates and the second stacked gate structures. Furthermore, the doping regions are disposed in the substrate under the first stacked gate structures, and the source/drain regions are disposed in the exposed substrate being at the outer side of the second stacked gate structures.

Please amend paragraphs [0012] as follows:

In another embodiment of the invention, a manufacturing method of NAND flash memory cell row is provided by the present invention. The method includes the following steps. First, a plurality of doping regions and a plurality of source/drain regions are formed in a substrate, wherein the source/drain regions are disposed at outer sides of the doping regions. Thereafter, a plurality of stacked gate structures are formed on the substrate. Each of the stacked gate structures disposed on the doping regions includes at least an erase gate, and some_of the stacked gate structures_are disposed at a distance from the doping regions and are disposed beside the source/drain regions and includes at least a select gate. Then, a tunnel oxide is formed on the substrate_to cover the substrate, the erase gate and the select gate surface. A plurality of floating gates are further formed between the stacked gate structures, a top surface of the floating gate is a_concave surface

and has a sharp edge, wherein an edge of the_concave surface is lower than the top surface of the erase gates. Then, an inter-gate dielectric layer is formed on the floating gates; and a plurality of control gates are formed on the inter-gate dielectric layer.

Please amend paragraphs [0020] as follows:

FIG. 1 is a cross-sectional view illustrating the structure of a NAND flash memory cell row according to the present invention. The memory cell rows illustrated in FIG. 1 have the same bit line 10, and each memory cell row has four memory cells. However, although the number of memory cells having the same bit line shown in FIG. 1 is only 4, the number of memory cells is not limited to 4. Instead, it is dependent on the design and requirement. For example, a bit line can be connected to a structure has 32 to 64_memory cells. Hereinafter, each drawing is illustrated and described by just using a memory cell row for simplification.

Please amend paragraphs [0021] as follows:

Referring to FIG. 1, the NAND flash memory cell row structure of the present invention includes at least a substrate 100, a plurality of first stacked gate structure 102, a tunnel oxide 104, a plurality of floating gate 106, a plurality of control gate 108, an inter-gate dielectric layer 110, doping regions 112, a plurality of second stacked gate structure 130_and source/drain regions 122. The first stacked gate structure 102 includes an erase gate dielectric layer 114, an erase gate 116_and a cap layer having an oxide layer 118a_and a dielectric layer 118b that are sequentially disposed on the surface of the substrate. The second stacked gate structure 130 includes a select gate dielectric layer 124,

a select gate 126_and a cap layer having an oxide layer 128a_and a dielectric layer 128b that are sequentially disposed on the surface of the substrate.

Please amend paragraphs [0024] as follows:

The stacked structure of the control gate_108 and the floating gate 106 is disposed between a plurality of the first stacked gate structure 102, and between the second stacked gate structure 130_and the_first stacked gate structure 102 adjacent to the structure 130. The material of the control gate 108 includes, for example but not limited to,_doped amorphous silicon. The floating gate 106 is disposed between each control gate 108_and the substrate 100, and each floating gate 106_has a concave surface 105. The concave surface 105 is faced to each control gate 108, and the edge 107 of the concave surface 105 is sharp, wherein the edge of the concave surface 105 is lower than the top surface of the erase gate 116. The stacked structures 109 constructed with the control gates 108_and the floating gates 106_are interlaced with the stacked gate structures 102.

Please amend paragraphs [0026] as follows:

The tunnel oxide layers 104 are disposed between each floating gates 106and the substrate 100, and between each floating gates 106_and the stacked gate structures 102. _The_material of the tunnel oxide layers 104 includes, for example but not limited to, a silicon oxide. The intergate dielectric layers 110 are disposed between the control gates 108 and the floating gates 106. The material of the inter-gate dielectric layer 110 includes, for example but not limited to, silicon oxide/silicon nitride/silicon oxide, silicon nitride/silicon oxide or silicon oxide/silicon nitride.

Please amend paragraphs [0027] as follows:

In the NAND flash memory cell row structure described above, since the floating gate 106 has a concave surface 105, the junction area between the floating gate 106_and the control gate 108 is increased. Thus the gate coupling ratio of the memory cell is also increased. Therefore, the working voltage of the operation is reduced and the operation speed and performance of the memory cell are increased.

Please amend paragraphs [0029] as follows:

[0029] Referring to FIG 2, each element having the same reference number with that in FIG 1 is referred to the corresponding element of the NAND flash memory cell of the present invention in FIG 1. Moreover, besides the floating gate 106_has a concave surface 105 to enhance the gate coupling ratio of the memory cell, the edge 107 of the concave surface 105 is sharp also to increase the erase speed of the memory cell due to the point discharge effect.

Please amend paragraphs [0031] as follows:

Referring to FIG 3A, a substrate 100 is provided. A device isolation structure has been formed on/in the substrate (not shown) to define an active region. Then, a plurality of doping regions 112_and a plurality of source/drain regions 122_are formed in the substrate 100, wherein the source/drain regions 122 are disposed at the outer side of the periphery of the doping regions 112. Moreover, when the substrate 100 is a p-type silicon substrate, generally a p-type well region 120_is formed in the substrate 100 before the doping regions 112_and the source/drain regions 122 are formed. Further, the depth of the p-type well region 120 is deeper than that of the doping regions 112.

Please amend paragraphs [0032] as follows:

Referring to FIG. 3B, a plurality of the first and second stacked gate structures 102, 130 is formed on the substrate 100, wherein each first stacked gate structure 102 _disposed on the doped region 112_has at least an erase gate 116. Moreover, each second stacked gate structure 130 that is disposed at a distance from the doping regions 112 and beside the source/drain regions 122 has at least a select gate 126. The first stacked gate structure 102 includes, for example but not limited to, an erase gate dielectric layer 114, an erase gate 116_and a cap layer having an oxide layer 118a_and a dielectric layer 118b. The second stacked gate structure 130 includes, for example but not limited to, a select gate dielectric layer 124, a select gate 126_and a cap layer having an oxide layer 128a_and a dielectric layer 128b. The step of forming the first and second stacked gate structures 102 and 130 includes that forming a first dielectric layer, a conductive layer, an oxide layer and a second dielectric layer on the substrate 100 sequentially. The material of the first dielectric layer includes, for example but not limited to, silicon oxide. The material of the conductive layer includes, for example but not limited to, doped amorphous silicon. The material of the second dielectric layer includes, for example but not limited to, silicon nitride. The method of forming the first dielectric layer on the substrate 100 includes a thermal oxidation method. The second dielectric layer, the oxide layer, the conductive layer and the first dielectric layer are patterned_to form the dielectric layer 118b, the oxide layer 118a, the erase gate 116_and the erase gate dielectric layer 114_and the dielectric layer 128b, the oxide layer 128a, the select gate 126_and the select gate dielectric layer 124. The oxide layers 118a and 128a_include, for example but not limited to, tetraethy- lorthosilicate (TEOS) oxide layer.

Please amend paragraphs [0033] as follows:

Then, referring to FIG 3C, a tunnel oxide layer 104 is formed on the substrate 100 to cover the surfaces_of the substrate 100, the erase gate 116_and the select gate 126. The material of the tunnel oxide layer 104 includes, for example but not limited to, a silicon oxide. The method of forming the tunnel oxide layer 104 includes, for example but not limited to, a thermal oxidation method. _Next, a conductive layer 103 is formed between the stacked gate structures 102 and 130, and then a portion of the constuctive layer 103 is removed to make the surface of the conductive layer 103_lower than the top surfaces of the first and second stacked gate structure 102 and 130. The method of removing a portion of the conductive layer 103 includes, for example but not limited to, an etch back method.

Please amend paragraphs [0034] as follows:

Next, referring to FIG 3D, the top surface of the conductive layer 103 is oxidized to form an oxide layer 111 on the top surface of the conductive layer 103. The method of oxidizing the top surface of the conductive layer 103 includes, for example but not limited to, a wet oxidation method. _Since the wet oxidation method will consume a portion of the conductive layer 103, the oxide layer 111_that is finally formed has a thick center and two sharp ends, which shapes like a "birds beak".

Please amend paragraphs [0035] as follows:

Then, referring to FIG 3E, the oxide layer 111 is removed (in comparison with FIG 3D) to form the floating gate 106, wherein the top surface is a concave surface 105 and the edge 107 of the top surface is sharp. The_edge of the concave surface 105 is

lower than the top surface of the erase gate 116. An inter-gate dielectric layer 110 is further formed on the floating gate 106, and a control gate 108 is formed on the inter-gate dielectric layer 110. The step of forming the control gate 108 includes, for example but not limited to, forming a conductive layer (not shown) on the substrate 100, and removing a portion of the conductive layer till the top surface of the dielectric layer 118b is exposed. The method of removing a portion of the conductive layer includes, for example but not limited to, an etch back method or a chemical mechanical polishing (CMP) method.

Please amend paragraphs [0038] as follows:

Accordingly, in the present invention, a surface of the floating gate of the NAND flash memory cell is provided as a concave surface. Since not only the junction area between the floating gate and the control gate is increased, the concave surface of the floating gate and the sharp_edge of the floating gate is also lower than the top surface of the erase gate. Therefore, the coupling ratio is enhanced. Thus, the erase speed and the performance of the memory cell are enhanced.

Please amend paragraphs [0039] as follows:

Moreover, in the present invention, the thermal oxidation process is provided for the manufacturing of the sharp edge of the floating gate. The oxide formed by the thermal oxidation is then removed to make the floating gate to have_a concave surface. Since the edge of the floating gate is sharp, the erase speed and the performance of the memory cell are enhanced.